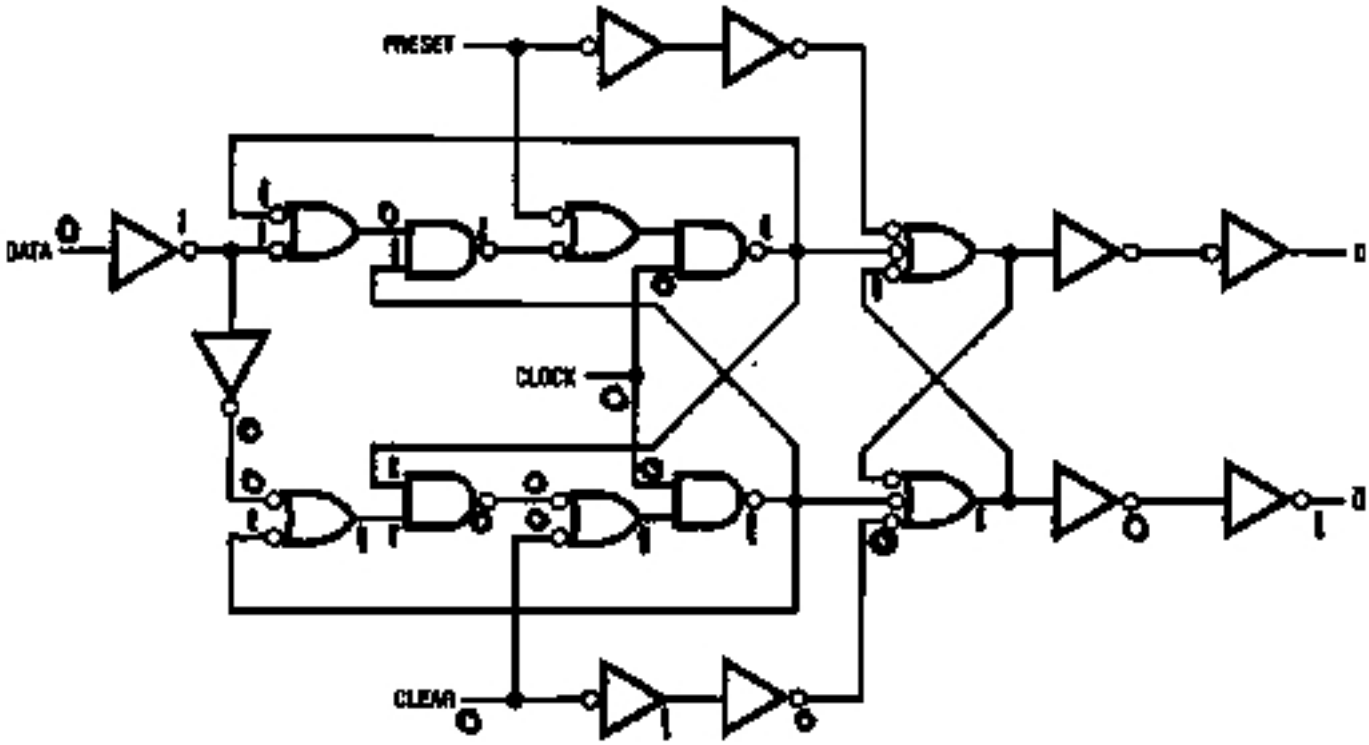
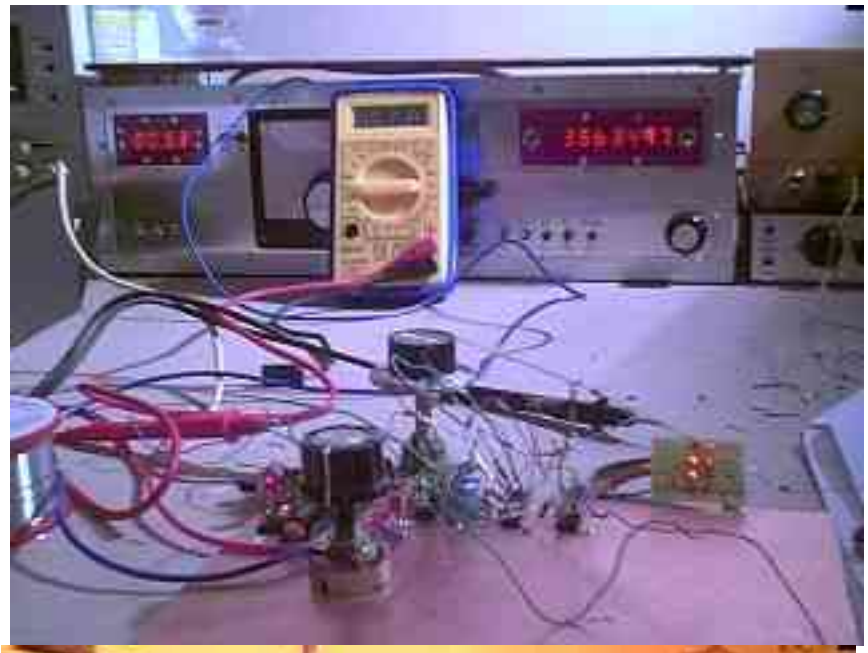


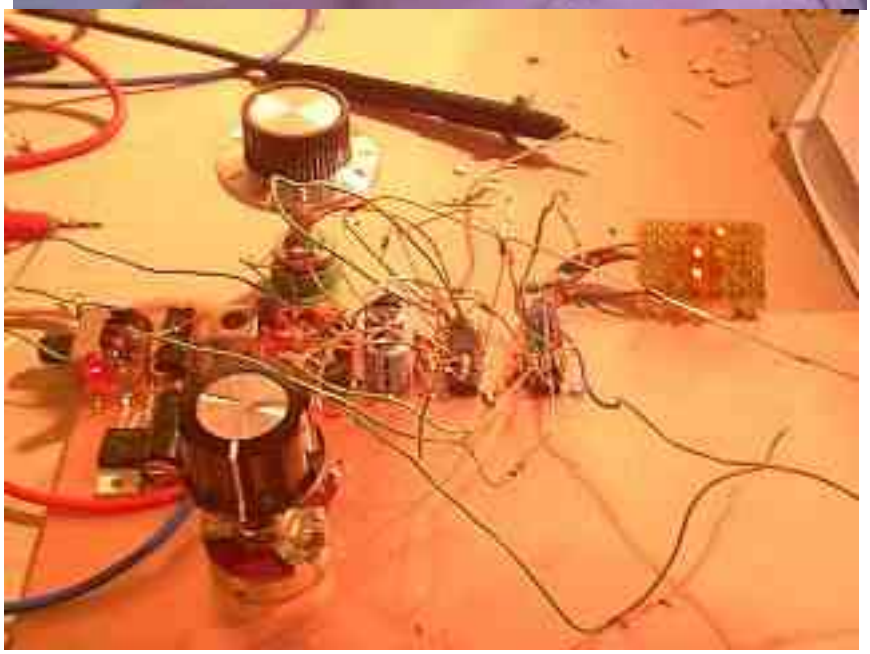

Two great conceptual leaps make this design possible. The first is the use of a much lower frequency crystal than normal, such that the 14 stages of division available in a single 74HC4060 used as oscillator and divider, are sufficient to obtain a low enough frequency for the Huff & Puff latch. The second is an innovative way to make one flip flop of the 74HC74 behave as an inverter, which can then be used to create an oscillator.

Usually the Huff & Puff stabiliser requires a latch to store the VFO state at precise intervals. A latch implies the use of a 74HC74 dual D-type flip flop IC. Somehow I had the idea that the spare flip flop in the IC might be configured to behave as an inverter. A study of the 74HC74 datasheet revealed that this is indeed the case: when D, CLK and /MR (clear) inputs are all held low, the signal presented to the /PR (preset) input is inverted and arrives at the Q output. The inverted output /Q remains always at 1 and cannot be used in this application.

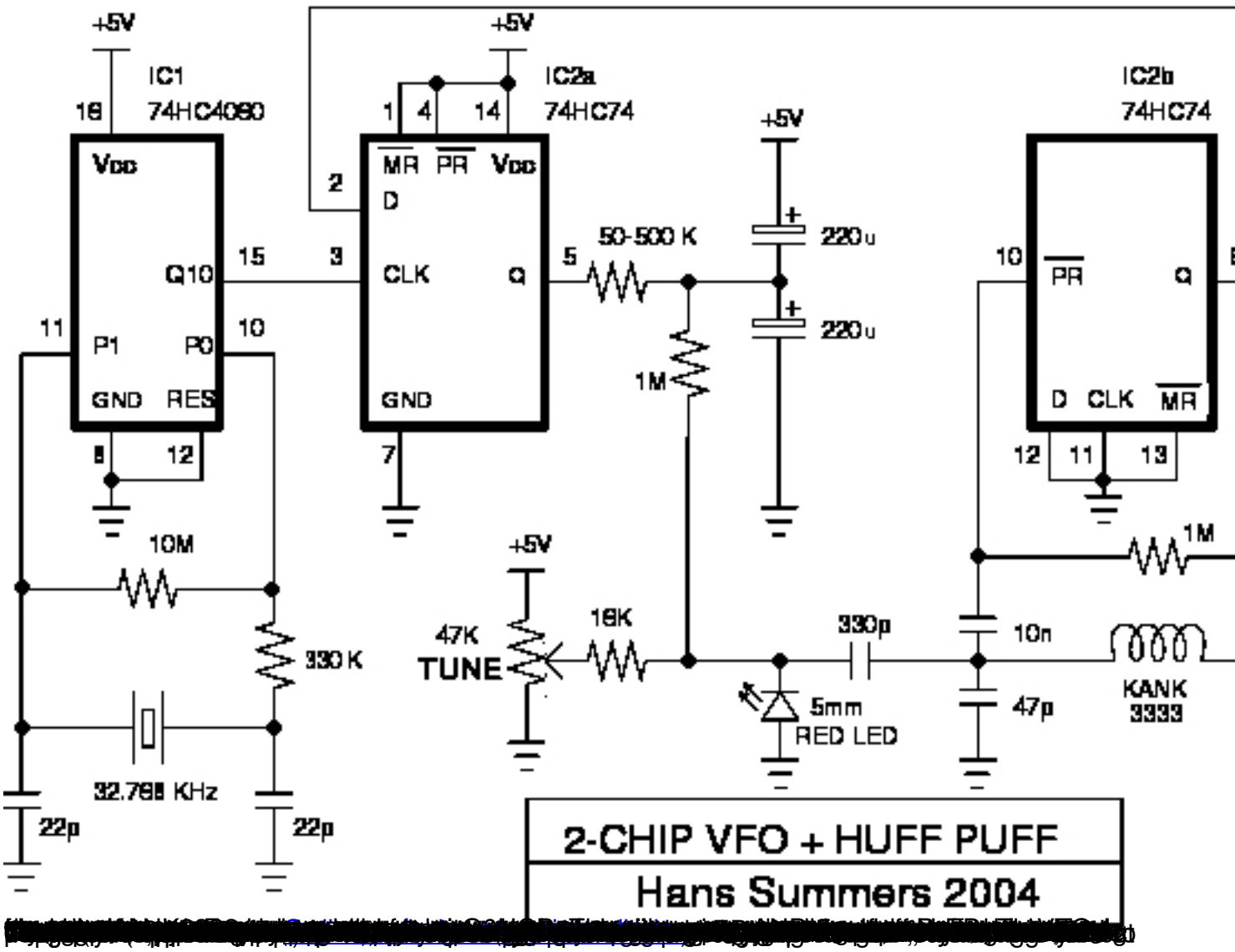
To the right, I have inserted the internal logic diagram of a 74HC74 flip flop, from the Fairchild Semiconductor datasheet. On this diagram, I started drawing 1's and 0's at the gate inputs and outputs, based on holding D, CLK and /MR at 0. It was reasonably easy to prove that under these conditions the only thing determining the state of the Q output, is the /PR input, via gates which behave effectively as five inverters in series. Therefore the flip flop as a whole behaves as an inverter! As soon as you have an inverter, you have a possible oscillator. I originally posted my idea to the Huff Puff oscillator forum and John G0UCP verified the design before I had time to build it myself. He made some modifications to my drawn oscillator section, which had been based on a circuit I had used before with a 74LS04 oscillator, in a 30m direct conversion recevier
. Thanks are therefore due to John for his oscillator modification, which I have used here.

Here are two pictures of my workbench during development of this project. By the time these photos were taken, it was already becoming a 3-chip combined VFO / Stabiliser and Frequency counter, as you will see in the next section. Note the spaghetti of wires over the "ugly" construction board. The potentiometer towards the rear is for VFO tuning. The 500K potentiometer in the foreground is used to experiment with different integrator settings (time constant). In the background, my Polyphase HF receiver with its homebuilt frequency counter, which is being used here to measure the VFO frequency NOT the receiver's own internal reception frequency.





And finally here is the circuit diagram. This circuit should in fact more accurately be known as a 1.5-chip Huff Puff Stabiliser combined with a 0.5-chip VFO. I use a 10nF decoupling capacitor across each chip's supply (not shown).


+5V
IC1
74HC4060
16
Vcc
Q10
15
11
P1
10
P0
GND
RES
8
12
10M
330 K
32.768 KHz
22p
22p
+5V
IC2a
74HC74
1
4
14
MR
PR
Vcc
2
D
CLK
Q
3
5
7
GND
50-500 K
+5V
220u
220u
1M
47K
TUNE
18K
+5V
IC2b
74HC74
10
PR
Q
D
CLK
MR
12
11
13
1M
330p
10n
47p
5mm
RED LED
KANK
3333
2-CHIP VFO + HUFF PUFF
Hans Summers 2004